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| 10/666,542 | 09/19/2003 | Thomas R. Apel | TRQ-12923 | 5554 |

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| EXAMINER | |
|---|---|
| SHINGLETON, MICHAEL B | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/666,542 | APEL, THOMAS R. | |
| | Examiner | Art Unit | |
| | Michael B. Shingleton | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-5,7-17 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7-17 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

An overview of the following rejection and observations of applicant's invention are offered so that the rejection can be better understood.

Applicant has amended the claims to resolve some 112 second paragraph issues and to change the wording of what essentially is the same claimed subject matter and this necessitated this new rejection. The examiner has stated many times that the broadest reasonable interpretation of the claims must be given. See MPEP 2111 and MPEP 904.01. The claims have this parallel amplifier arrangement with the various delays, "impedance inverter" and arrangement that control the activation of the selected amplifier elements. While the applicant may disagree and read too much of the specification into the claim(s) that are not there, the prior art to Taniguchi will read on the bulk of the claimed structure. Since the bulk of the claims will read on the Taniguchi reference and should applicant believe that there is structure that is not present in Taniguchi then clearly what that structure is exactly is ambiguous or ambiguously presented in the claims. Halliburton Energy Services, Inc v M-I LLC, Fed. Cir, 2007-1149. states: **"[b]ecause claims delineate the patentee's right to exclude, the patent statute requires that the scope of the claims be sufficiently definite to inform the public of the bounds of the protected invention, i.e., what subject matter is covered by the exclusive rights of the patent. Otherwise, competitors cannot avoid infringement, defeating the public notice function of the patent claims**." As recited in the above Halliburton decision the court says "**We note that the patent drafter is in the best position to resolve ambiguity in the patent claims, and it is highly desirable that the patent examiners demand that applicants do so in appropriate circumstances so that the patent can be amended during prosecution rather than attempting to resolve the ambiguity in litigation**.". Also note that the Halliburton decision relates to the situation where applicant is very specific as to specific limitations on structure that has already been "seen" and then the claims seems to recite functional language "at the exact point of novelity". Many times these types of claims are indefinite. Again the Halliburton decision states: Claims could be held indefinite "**when the inventor is painstaking when he recites what has already been seen, and then uses conveniently functional language at the exact point of novelty"**. The Halliburton decision recited two Supreme Court cases that "identified the dangers of using only functional claim limitations to distinguish the claimed invention from the prior art" and these are General Electric, 304 U.S. at 371 and United Carbon, 317 U.S. at 234. What is needed in this application is clear limitations to positive structure in the claims that can distinguish the claimed invention over the prior art, i.e. the claimed positive limitations to structure will not read on the prior art.

The other main issue deals with the turning on and off the various amplifier elements in a parallel combination of amplifier elements to control the power level transmitted to the load(s). The examiner has cited the Apel reference and note that there is a signal to control the turning on and off of the stage 222 so that during high power both 221 and 222 stages are on and during low power only stage 221 is on (See the paragraph bridging columns 2 and 3.). From the examiner's experience there are many other references that teach controlling the turning on/off of the various amplifier(s) to control the power delivered to the load in an arrangement of parallel connected amplifiers/stages. This concept is very old and it is not necessary to cite each and every reference to show this. Thus the examiner has to respectfully disagree with applicant that such would not be an obvious addition to the prior art of Taniguchi. Plus an argument that it may not work well in Taniguchi is not an argument that it would not be obvious. The examiner contends that it will work and applicant must prove that it would not work at all which will be impossible in this case. Again applicant is in the best position to present non-ambiguous limitations of real structure in the claims to make it absolutely clear to the public the bounds of the protected invention so that competitors can avoid infringement and currently that does not exist. Without clear limitations to structure the public may invest many dollars and make an invention that they believe

and would have good reason to believe does not infringe due to the ambiguous nature of the claim. This does not promote the useful arts and sciences but only repeats and spends unnecessary resources on the same stuff. And again the examiner can read the claimed subject matter on the prior art of record which includes what the reference taken together teach or suggest to one of ordinary skill in the art, See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986), and although this reading may not be what applicant had in mind, it is applicant that is to make sure that the claim structure is clear and not ambiguous so that the attempt to resolve the ambiguous nature of the claims will not in litigation as the above caselaw makes clear.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi et al. 5,162,756 (Taniguchi) in view of Holt and Apel US 6,894,561 (Apel).

Fig. 2
PRIOR ART

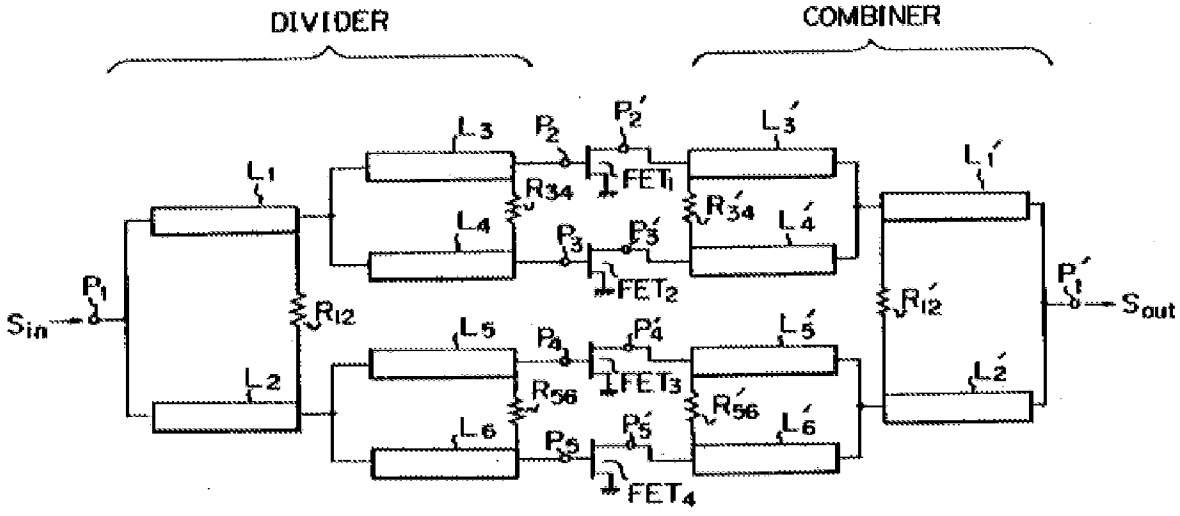

Figure 2 (Taniguchi)

Figure 2 of Taniguchi discloses a power amplifier circuit. Note that the goal of these circuits of Taniguchi is to "obtain a high power high frequency signal" (See column 3, around line 59) and thus these circuits are power amplifier circuits. Taniguchi includes a first amplifier "subsection" $L_3$ and $FET_1$ (Herein and throughout referred to just as the first amplifier.) that is configured to receive an input signal that is the unmarked signal at the node that directly connects elements $L_1$, $L_3$, and $L_4$. Note that the first amplifier receives this signal through element $L_3$. This is only giving the broadest reasonable interpretation to the claims consistent with the specification. See MPEP 904.01. The first amplifier clearly provides a "first" output signal. Element $L_4$ of Taniguchi is a first delay element that introduces a delay to the input signal and applies this to the input of a "second" amplifier "subsection" $FET_2$ (Herein and throughout referred to just as the second amplifier.). This second amplifier clearly has an output signal and provides a "first" delayed output signal to the node directly connecting elements $L_3$', $L_4$' and $L_1$'. The top of page 9, of applicant's specification clearly sets forth that an impedance inverter can be a quarter wavelength transmission line. Thus all the quarter wavelength lines of Taniguchi are "impedance inverters" as set forth by applicant and is in accordance with applicant's application. These impedance inverters of Taniguchi are in accordance with applicant's specification provides the "impedance inversion". Thus the impedance/delay element $L_3$'also introduces a second delay to the first output signal thereby creating a second delayed output signal. The node directly connecting elements $L_3$', $L_4$' and $L_1$' and the node directly connecting elements $L_5$', $L_6$' and $L_2$' in combination with the node that directly connects elements $L_1$' and $L_2$' provides the means for combining the first and second delayed output signals that ultimately provides the high frequency amplified output signal $S_{out}$. This output signal is provided on the output terminal "$P_1$' ". Taniguchi is silent on showing the bias circuit and supply circuit or what applicant calls "level control circuit" in claims like claim 1 for example that biases the first and second amplifiers to operate in the saturation range, i.e. non-linear classes of operation. Applicant should note that while Taniguchi is silent on the bias circuit or "level control circuit". As is known to those of ordinary skill in the art, Taniguchi inherently must have a bias circuit and power supply circuit because this is a necessary circuit needed so that the amplifier(s) can operate.

The structure indicated above clearly provides for the claimed method of the claims indicated at the beginning of this rejection except for as indicated above Taniguchi is silent on providing a bias control circuit/level control circuit that biases the amplifiers such that non-linear operation is obtained.

Holt teaches that it is well known to provide a bias circuit and power supply circuit so that the

amplifier can operate, i.e. amplify and to choose the bias level, so that a non-linear operation is obtained. Note that if a bipolar is used the power supply would be to the collector. Nonlinear operation results in the more efficient use of a amplifier for the transistor is not on all the time, Thus, the selection of the class of operation is merely the selection of a result effective variable that determines the energy consumption of the amplifier.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Taniguchi with a bias control circuit(s)/power supply circuits that biases and supplies power to the first and second amplifiers such that non-linear operation is obtained for these amplifiers because, as the reference is silent on the exact biasing/power supply circuit one of ordinary skill in the art would have been motivated to use any conventional art recognized equivalent biasing circuit and power supply circuit therewith such as non-linear biasing/power supply arrangements of Holt. In addition, one of ordinary skill would have been motivated to do so because providing a bias circuit to cause operation in the non-linear region has the added advantage of providing the most energy efficient amplification of the input signal as taught by Holt.

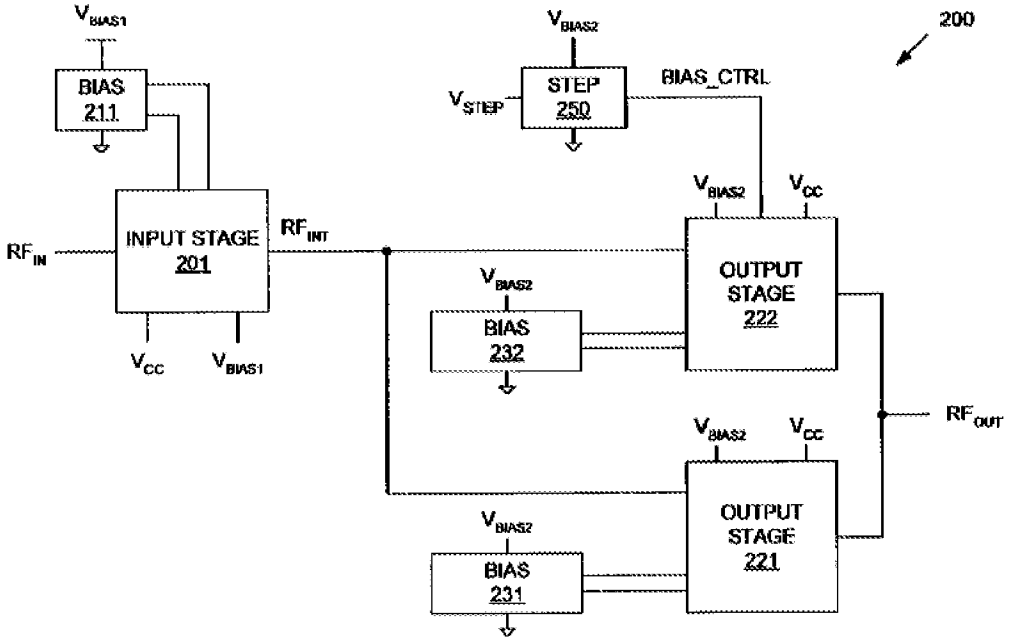


FIG. 2

Figure 2(Apel)

Figure 2 of Apel teaches one way to have a multi-channel amplifier arrangement provide for low power and high power modes. This includes the providing of a "bias control circuit" 231, 232, 250 that enables the first amplifier 221 when the "level control signal" $V_{STEP}$ is set for a low power mode and which enables the second amplifier 222 when the "level control signal" is set for a high power mode.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the combination of Taniguchi and Holt with a bias control circuitry such as that of Apel so as to enable the first amplifier during a low power mode indicated by a level control signal and enable both the first and second amplifiers when the level control signal indicates a high power mode. Therefore the multi-channel amplifier arrangement can be made to provide more than one power level output mode as taught by Apel.

Note that the selection of the bias points of the bias circuits in the combination of Taniguchi, Holt and Apel results in the level control circuit, i.e. the unshown circuit that provides the level control signal $V_{STEP}$, to allow for the level control circuit to cause the first and second amplifiers to operate in the saturation mode when these amplifiers are enabled.

With respect to claims like claims 11 and 12 the delay circuits of Taniguchi are quarter wavelength lines. It is well known in the art that a delay line can be composed of an inductor and one or more capacitors. These are art-recognized equivalents. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the inductor with one or more capacitors for the transmission delay lines of Taniguchi since the examiner takes Official Notice of the equivalence of the inductor with at one or more capacitors and the transmission delay line for use in the circuitry art and the selection of any of these known equivalents to provide delay/impedance inversion would be within the level of ordinary skill in the art.

As it relates to claims like claims 13 and 18, bipolar/heterojunction elements are well known to be art recognized equivalents to that of FETs. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted bipolar transistors for the FET transistors of Taniguchi since the examiner takes Official Notice of the equivalence of the bipolar/heterojunction element and FET element for use in the circuitry art and the selection of any of these known equivalents to provide amplification would be within the level of ordinary skill in the art. Note that the step/structure of applying a first output level control signal to a collector of the first amplifier "subsection" would be an obvious consequence of the combination made obvious above.

Claims 2-4, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi

et al. 5,162,756 (Taniguchi) in view of Holt and Apel as applied to claims 1, and 11-16 above, and further in view of Cheng et al. 2002/0190790 (Cheng).

All the reasoning as applied in the rejection of claims 1, 6, and 11-16 and the following: Taniguchi fails to describe using the biasing arrangement to disable one or more of the amplifiers in accordance with the power level one wants to obtain and Apel is silent on the structural details i.e. the specific circuit structure (The switches, transistors, etc. necessary to perform the enabling and disabling of the biasing arrangement taught by Apel.).

Cheng teaches that one can selectively supply the bias voltages each of the parallel-connected amplifiers so as to control the operation of these amplifiers, i.e. whether they are on or off. This controls the amount of power delivered to the load (See page "4" paragraph numbered "[0037]".),

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the bias control circuit of Taniguchi in view of Apel and Holt so as to selectively control the bias voltages to the respective amplifiers of the arrangement thereby providing not only low and high power modes but a mode of no power wherein all the amplifying devices are disabled. One of ordinary skill would have been motivated to do so as to control the amount of output power as taught by Cheng.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi, Holt, Apel and Cheng as applied to claims 2-4, 17 and 20 above, and further in view of Atwater 4,189,732 (Atwater).

Taniguchi, Holt and Cheng fail to disclose the power supply arrangement as claimed. Holt is silent on the exact power supply circuit.

The only Figure of Atwater discloses a well-known circuit for providing a power supply voltage to an amplifier. This circuit includes a transistor 12, and an inductor 33 connected in series between the power supply voltage at 10 and the amplifier 46. This provides the "right" power supply level to the amplifier without supplying excess power to the amplifier that would have to be dissipated by the amplifier (See column 4, around line 44.).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have employed the circuit like Atwater for each of the amplifier circuits in the combination of Taniguchi, Cheng and Holt because, as these references are silent on the exact power supply circuit one of ordinary skill in the art would have been motivated to use any art-recognized equivalent power supply circuit for the amplifiers such as the conventional power supply circuit shown by Atwater. Additionally, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to provide a power supply circuit like that of Atwater for each amplifier in the combination of Taniguchi, Cheng and Holt for one of ordinary skill in the art would have been motivated to do so as to provide a correct amount of power while preventing excess power to the amplifiers as taught by Atwater.

Note that just like in applicant's disclosed invention the term ramp is to signify the ramping of the voltage when the supply voltage is supplied to the amplifier. This is caused by the inductor and thus when the power is first applied to the power supply 11 of Atwater the voltage applied to the amplifier is in the form of a ramp. Therefore it is an obvious consequence of the combination made obvious above that the first and second output level control signals are ramp signals as meant by applicant. Also note that the claimed specific inductor/transistor combinations are an obvious consequence of the above combination.

Claims 5, 7-10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi, Holt and Apel as applied to claims 1 and 11-16 above, and further in view of Atwater 4,189,732 (Atwater).

Taniguchi fails to disclose the power supply arrangement as claimed. Holt is silent on the exact power supply circuit.

The only Figure of Atwater discloses a well-known circuit for providing a power supply voltage to an amplifier. This circuit includes a transistor 12, and an inductor 33 connected in series between the power supply voltage at 10 and the amplifier 46. This provides the "right" power supply level to the amplifier without supplying excess power to the amplifier that would have to be dissipated by the amplifier (See column 4, around line 44.).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have employed the circuit like Atwater for each of the amplifier circuits in the combination of Taniguchi and Holt because, as these references are silent on the exact power supply circuit one of ordinary skill in the art would have been motivated to use any art-recognized equivalent power supply circuit for the amplifiers such as the conventional power supply circuit shown by Atwater. Additionally, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a power supply circuit like that of Atwater for each amplifier in the combination of Taniguchi and Holt for one of ordinary skill in the art would have been motivated to do so as to provide a correct amount of power while preventing excess power to the amplifiers as taught by Atwater.

Note that just like in applicant's disclosed invention the term ramp is to signify the ramping of the voltage when the supply voltage is supplied to the amplifier. This is caused by the inductor and thus when the power is first applied to the power supply 11 of Atwater the voltage applied to the amplifier is in the form of a ramp. Therefore it is an obvious consequence of the combination made obvious above that

the first and second output level control signals are ramp signals as meant by applicant. Also note that the claimed specific inductor/transistor combinations are an obvious consequence of the above combination.

***Response to Arguments***

Applicant's arguments with respect to the claims of record have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker, can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
May 11, 2008

/Michael B. Shingleton/
Michael B Shingleton
Primary Examiner
Group Art Unit 2815